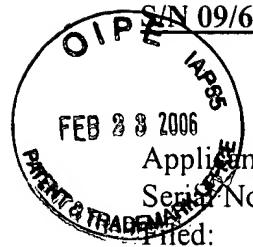


O I P S/N 09/698,188

PATENT



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Thomas E. Burton et al. Examiner: Larry Donaghue  
Serial No.: 09/698,188 Group Art Unit: 2154  
Filed: October 30, 2000 Docket: 884.983US1  
Title: HOST-FABRIC ADAPTER HAVING HARDWARE ASSIST ARCHITECTURE  
AND METHOD OF CONNECTING A HOST SYSTEM TO A CHANNEL-  
BASED SWITCHED FABRIC IN A DATA NETWORK  
Assignee: Intel Corporation Customer Number: 21186

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

MS Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants have included the fee of \$180.00 as set forth in 37 C.F.R. §1.17(p). Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Customer No.: 21186

Serial No.: 09/698,188

Filing Date: October 30, 2000

Title: HOST-FABRIC ADAPTER HAVING HARDWARE ASSIST ARCHITECTURE AND METHOD OF CONNECTING A HOST SYSTEM TO A CHANNEL-BASED SWITCHED FABRIC IN A DATA NETWORK

Assignee: Intel Corporation

Page 2  
Dkt: 884.983US1 (INTEL)

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

THOMAS E. BURTON ET AL.

By their Representatives,

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Date FEB. 21/2006

By Robert Madden  
Robert Madden  
Reg. No. 57,521

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 21st day of February, 2006.

Name

Amy Moriarty

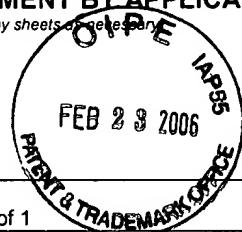
Signature

A. J.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known	
<b>Application Number</b>	09/698,188
<b>Filing Date</b>	October 30, 2000
<b>First Named Inventor</b>	Burton, Thomas
<b>Group Art Unit</b>	2154
<b>Examiner Name</b>	Donaghue, Larry

Sheet 1 of 1

Attorney Docket No: 884.983US1

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**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		TORRES, D. , et al., "A new bus assignment in a designed shared bus switch fabric", <u>Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, ISCAS '99, Volume 1</u> , (1999),423-426	

**EXAMINER****DATE CONSIDERED**